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FROM: Peter Yim
Reg. No. 44,417**DATE:** March 9, 2006

Number of pages with cover page:	9	
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U.S. Patent Application Serial No. 10/799,061
 For: SELECTING DIE PLACEMENT ON A SEMICONDUCTOR
 WAFER TO REDUCE TEST TIME
 By: Eitan CADOURI
 Our Reference: 52432-20012.00

Attached is the following:

1. Transmittal (1 Page)
2. Amendment Under 37 CFR 1.116 (7 pages)

sf-2093267

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TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>		Application Number 10/799,061
Total Number of Pages in This Submission 8		Filing Date March 12, 2004
		First Named Inventor Eitan CADOURI
		Group Art Unit 2829
		Examiner Name J. Hollington
		Attorney Docket Number 524322001200

ENCLOSURES (check all that apply)

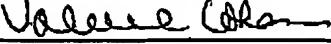
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers (for an Application)	<input type="checkbox"/> After Allowance Communication to Group
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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Status Letter
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below)
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	
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<input type="checkbox"/> Response to Missing Parts/ Incomplete Application		
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		
Remarks		

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Firm or Individual Name	MORRISON & FOERSTER LLP (Customer Number 20872) Peter J. Yim - Reg. No. 44,417
Signature	
Date	March 9, 2006

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Dated: March 9, 2006

Signature:  (Valerie Cohan)

sf-2093497

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REPLY UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER 2800Docket No.: 524322001200
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Dated: March 9, 2006 Signature: Valerie (Valerie Cohen)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Eitan CADOURI

Application No.: 10/799,061

Confirmation No.: 6747

Filed: March 12, 2004

Art Unit: 2829

For: SELECTING DIE PLACEMENT ON A
SEMICONDUCTOR WAFER TO REDUCE
TEST TIME

Examiner: J. Hollington

AMENDMENT UNDER 37 C.F.R. 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Final Office Action dated January 9, 2006 (Paper No. 20060106), for which a response is due on April 9, 2006. Accordingly, this response is timely filed. Additionally, this response is filed within two months of the mailing date of the Final Office Action and therefore qualifies for expedited review. Reconsideration and allowance of the pending claims, as amended, in light of the remarks presented herein are respectfully requested.

sf-2068544